In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) An apparatus for bridging video formats from an incoming video stream, the input video stream characterized by an input frame rate, an input number of pixels per line, an input number of lines per frame, an input number of active pixels per line and an input number of active lines per frame; for display on a output display device, comprising:

an input for an input video stream;

an output for an output video stream for the output display;

a buffer storing input pixels at the input clock rate, and outputting pixels for the output video stream;

a reference clock source, and an output clock generator, responsive to the reference clock source, generating an output clock signal for the display, and using the clock signal producing a pixel clock determining pixel timing for the output video stream, a horizontal synchronization clock determining a line length in the output video stream, and a vertical synchronization clock determining a frame length in the output video stream; and

bridge logic which produces the output video stream having an output frame rate matching the input frame rate, in which an output frame has at least one of a variable number of pixels per line within the output frame, and a variable number of lines per frame among output frames in the output video stream.

2. (currently amended) An apparatus for bridging video formats from an incoming video stream, the input video stream characterized by an input frame rate, an input number of pixels per line, an input number of lines per frame, an input number of active pixels per line and an input number of active lines per frame; for display on a output display device, comprising:

an input for an input video stream;

an output for an output video stream for the output display;

a buffer storing input pixels at the input clock rate, and outputting pixels for the output video stream;

a reference clock source, and an output clock generator, responsive to the reference clock source, generating an output clock signal for the display, and using the clock signal producing a pixel clock determining pixel timing for the output video stream, a horizontal synchronization clock determining a line length in the output video stream, and a vertical synchronization clock determining a frame length in the output video stream; and

bridge logic which produces the output video stream having an output frame rate matching the input frame rate, ~~The apparatus of claim 1,~~ wherein said bridge logic produces a residue line within the output frame, the residue line having a length less than a minimum line length, and distributes said residue line using a variable number of pixels per line within the output frame.

3. (currently amended) An apparatus for bridging video formats from an incoming video stream, the input video stream characterized by an input frame rate, an input number of pixels per line, an input number of lines per frame, an input number of active pixels per line and an input number of active lines per frame; for display on a output display device, comprising:

an input for an input video stream;

an output for an output video stream for the output display;

a buffer storing input pixels at the input clock rate, and outputting pixels for the output video stream;

a reference clock source, and an output clock generator, responsive to the reference clock source, generating an output clock signal for the display, and using the clock signal producing a pixel clock determining pixel timing for the output video stream, a horizontal synchronization clock determining a line length in the output video stream, and a vertical synchronization clock determining a frame length in the output video stream; and

bridge logic which produces the output video stream having an output frame rate matching the input frame rate, ~~The apparatus of claim 1,~~ wherein said bridge logic produces a residue line within the output frame, the residue line having a length less than a minimum line length, and accumulates said residue lines across multiple output frames until a number residue pixel clock cycles accumulated is greater than a minimum number of pixels per line, and then adds an extra line to an output frame in the output video stream.

4. (currently amended) An apparatus for bridging video formats from an incoming video stream, the input video stream characterized by an input frame rate, an input number of pixels per line, an input number of lines per frame, an input number of active pixels per line and an input number of active lines per frame; for display on a output display device, comprising:

an input for an input video stream;

an output for an output video stream for the output display;

a buffer storing input pixels at the input clock rate, and outputting pixels for the output video stream;

a reference clock source, and an output clock generator, responsive to the reference clock source, generating an output clock signal for the display, and using the clock signal producing a pixel clock determining pixel timing for the output video stream, a horizontal synchronization clock determining a line length in the output video stream, and a vertical synchronization clock determining a frame length in the output video stream; and

bridge logic which produces the output video stream having an output frame rate matching the input frame rate, ~~The apparatus of claim 1,~~ in which the bridge logic matches the input frame rate to the output frame rate by determining a number of lines plus a number of pixels in the input video stream as an input delay, counting the input delay, and issuing a force signal when the input delay is reached, and starting a first active line in a frame in the output video stream synchronized with the output clock signal, in a next line after the force signal.

5. (original) The apparatus of claim 4, wherein said predetermined input delay is computed periodically to account for variations in the input clock.

6. (currently amended) An apparatus for bridging video formats from an incoming video stream, the input video stream characterized by an input frame rate, an input number of pixels per line, an input number of lines per frame, an input number of active pixels per line and an input number of active lines per frame; for display on a output display device, comprising:

an input for an input video stream;

an output for an output video stream for the output display;

a buffer storing input pixels at the input clock rate, and outputting pixels for the output video stream;

a reference clock source, and an output clock generator, responsive to the reference clock source, generating an output clock signal for the display, and using the clock signal producing a pixel clock determining pixel timing for the output video stream, a horizontal synchronization clock determining a line length in the output video stream, and a vertical synchronization clock determining a frame length in the output video stream; and

bridge logic which produces the output video stream having an output frame rate matching the input frame rate, ~~The apparatus of claim 1,~~ wherein said bridge logic determines a normalized distance between the input video stream and the output video stream at a position in an output line, and adjusts the number of pixels per output line in response to the normalized distance.

7. (original) The apparatus of claim 6, wherein the logic increases the number of pixels per line if the normalized distance is less than a minimum distance, decreases the number of pixels per line if the normalized distance is greater than a maximum distance, else does not change the number of pixels per line.

8. (currently amended) An apparatus for bridging video formats from an incoming video stream, the input video stream characterized by an input frame rate, an input number of pixels per line, an input number of lines per frame, an input number of active pixels per line and an input number of active lines per frame; for display on a output display device, comprising:

an input for an input video stream;

an output for an output video stream for the output display;

a buffer storing input pixels at the input clock rate, and outputting pixels for the output video stream;

a reference clock source, and an output clock generator, responsive to the reference clock source, generating an output clock signal for the display, and using the clock signal producing a pixel clock determining pixel timing for the output video stream, a horizontal synchronization clock determining a line length in the output video stream, and a vertical synchronization clock determining a frame length in the output video stream; and

bridge logic which produces the output video stream having an output frame rate matching the input frame rate, ~~The apparatus of claim 1,~~ wherein said output clock source dithers the output clock rate.

9. (currently amended) The apparatus of claim 1, wherein said output clock generator ~~source~~ comprises a phase locked loop for synchronization with the input clock, and a frequency divider.

10. (currently amended) An apparatus for bridging video formats from an incoming video stream, the input video stream characterized by an input frame rate, an input number of pixels per line, an input number of lines per frame, an input number of active pixels per line and an input number of active lines per frame; for display on a output display device, comprising:

an input for an input video stream;

an output for an output video stream for the output display;

a buffer storing input pixels at the input clock rate, and outputting pixels for the output video stream;

a reference clock source, and an output clock generator, responsive to the reference clock source, generating an output clock signal for the display, and using the clock signal producing a pixel clock determining pixel timing for the output video stream, a horizontal synchronization clock determining a line length in the output video stream, and a vertical synchronization clock determining a frame length in the output video stream; and

bridge logic which produces the output video stream having an output frame rate matching the input frame rate, ~~The apparatus of claim 1,~~ wherein said bridge logic includes resources to set a lower bound input delay and an upper bound input delay, wherein the lower and upper bound input delays are respective numbers of lines plus numbers of pixels in the input video stream after a fixed point; to output a first active line in a frame of the output video stream after a back porch number of lines in the output video stream after an output vertical synchronization clock cycle; to insert a front porch number of lines in the output video stream after a last active line in said frame of the output video stream; and to adjust the number of front porch lines if the first active line in said frame in the output video stream is outputted before the lower bound input delay or after the upper bound input delay.

11. (original) The apparatus of claim 1, wherein said bridge logic includes resources supporting a plurality of bridging processes, and resources by which a user enables and disables selected bridging processes in the plurality of bridging processes.

12. (original) A method for bridging an input video stream to an output video stream for a display; comprising:

generating an output clock signal for the display, and using the output clock signal producing a pixel clock determining pixel timing for the output video stream, a horizontal synchronization clock determining a line length in the output video stream, and a vertical synchronization clock determining a frame length in the output video stream;

causing an output frame supplied to the display using said output clock signal to have a period substantially the same as a frame in the input video stream;

determining a number of pixel clock cycles in a residue line within the output frame; and

if the number of pixels clock cycles in the residue line is less than a minimum line length, then distributing the pixel clock cycles of the residue line to other lines in the frame, by providing a number of lines having a first number of pixel clock cycles, and a number of lines having a second number of pixel clock cycles different than the first number.

13. (original) The method of claim 12, wherein the first number and the second number differ by one pixel clock cycle.

14. (original) The method of claim 12, wherein the first number and the second number differ by more than one pixel clock cycle.

15. (original) The method of claim 12, wherein said causing includes determining a number of lines plus a number of pixels in the input video stream as an input delay, counting the input delay after a fixed point, and issuing a force signal when the input delay is reached, and starting a first active line in a frame in the output video stream synchronized with the output clock signal, in a next line after the force signal.

16. (original) The method of claim 12, wherein the output video frame has a non-integer average number of pixels per line.

17. (original) The method of claim 15, wherein the number of pixels in the input delay is non-zero.

18. (original) The method of claim 12, wherein the input video frame has a ratio of a number of lines per frame to a number of active lines per frame, and including adjusting said ratio by making normally inactive lines into active blank lines.

19. (currently amended) A method for bridging an input video stream to an output video stream for a display; comprising:

generating an output clock signal for the display, and using the output clock signal producing a pixel clock determining pixel timing for the output video stream, a horizontal synchronization clock determining a line length in the output video stream, and a vertical synchronization clock determining a frame length in the output video stream;

causing an output frame supplied to the display using said output clock signal to have a period substantially the same as a frame in the input video stream by determining a number of lines plus a number of pixels in the input video stream as an input delay, counting the input delay in the input video stream after a fixed point, and issuing a force signal when the input delay is reached, and starting a first active line in a frame in the output video stream synchronized with the output clock signal, in a next line after the force signal.

20. (original) The method of claim 19, wherein the number of pixels in the input delay is non-zero.

21. (currently amended) A method for bridging an input video stream to an output video stream for a display; comprising:

generating an output clock signal for the display, and using the output clock signal producing a pixel clock determining pixel timing for the output video stream, a horizontal

synchronization clock determining a line length in the output video stream, and a vertical synchronization clock determining a frame length in the output video stream;

causing an output frame supplied to the display using said output clock signal to have a period substantially the same as a frame in the input video stream; and

determining a number of frames in a set of frames in the output video stream in which a number of pixel clock cycles in a residue lines of the frames in the set reaches a minimum number, and then inserting an extra line in one frame of said set of frames.

22. (original) The method of claim 21, wherein said determining and inserting includes:

accumulating pixel clock cycles from residue lines within output frames; and

when the accumulated number of pixel clock cycles is greater than a minimum number for a line in the output video frame, inserting an extra line in the output video frame and restarting said accumulating.

23. (original) The method of claim 21, wherein the set of frames has a non-integer average number of lines per frame.

24. (original) The method of claim 21, wherein said causing and determining includes:

setting an lower bound input delay and an upper bound input delay, wherein the lower and upper bound input delays are respective numbers of lines plus numbers of pixels in the input video stream after a fixed point;

outputting a first active line in a frame of the output video stream after a back porch number of lines in the output video stream after an output vertical synchronization clock cycle;

inserting a front porch number of lines in the output video stream after a last active line in said frame of the output video stream; and

adjusting the number of front porch lines if the first active line in said frame in the output video stream is outputted before the lower bound input delay or after the upper bound input delay.

25. (original) The method of claim 24, wherein the number of pixels in one of the lower bound input delay and upper bound input delay is non-zero.

26. (currently amended) A method for bridging an input video stream to an output video stream for a display; comprising:

generating an output clock signal for the display, and using the output clock signal producing a pixel clock determining pixel timing for the output video stream, a horizontal synchronization clock determining a line length in the output video stream, and a vertical synchronization clock determining a frame length in the output video stream;

setting an lower bound input delay and an upper bound input delay, wherein the lower and upper bound input delays are respective numbers of lines plus numbers of pixels in the input video stream;

outputting a first active line in a frame of the output video stream after a back porch number of lines in the output video stream after an output vertical synchronization clock cycle;

inserting a front porch number of lines in the output video stream after a last active line in said frame of the output video stream; and

adjusting the number of front porch lines if the first active line in said frame in the output video stream is outputted before the lower bound input delay or after the upper bound input delay.

27. (original) The method of claim 26, wherein the number of pixels in one of the lower bound input delay and upper bound input delay is non-zero.

28. (currently amended) A method for bridging an input video stream to an output video stream for a display; comprising:

generating an output clock signal for the display, and using the output clock signal producing a pixel clock determining pixel timing for the output video stream, a horizontal synchronization clock determining a line length in the output video stream, and a vertical synchronization clock determining a frame length in the output video stream;

counting input active lines and pixels to determine a position in the input frame and output active lines and pixels to determine a position in the output frame;

during outputting of active output lines, determining a normalized distance between the position in the input frame and the position in the output frame; and

adjusting the number of pixels per line according to the normalized distance.

29. (original) The method of claim 28, including determining the normalized distance at the beginning of output active lines.

30. (original) The method of claim 28, including adjusting the number of pixels per line at the end of output active lines.

31. (original) The method of claim 28, including:

setting an lower bound input delay and an upper bound input delay, wherein the lower and upper bound input delays are respective numbers of lines plus numbers of pixels in the input video stream;

outputting a first active line in a frame of the output video stream after a back porch number of lines in the output video stream after an output vertical synchronization clock cycle;

inserting a front porch number of lines in the output video stream after a last active line in said frame of the output video stream; and

adjusting the number of front porch lines if the first active line in said frame in the output video stream is outputted before the lower bound input delay or after the upper bound input delay.

32. (currently amended) The method of clam 28, including:

causing an output frame supplied to the display using said output clock signal to have a period substantially the same as a frame in the input video stream; and

determining a number of frames in a set of frames in the output video stream in which a number of pixel clock cycles in a residue lines of the frames in the set reaches a minimum number, and then inserting an extra line in one frame of said set of frames.

33. (original) The method of claim 32, wherein said determining and inserting includes:

accumulating pixel clock cycles from residue lines within output frames; and

when the accumulated number of pixel clock cycles is greater than a minimum number for a line in the output video frame, inserting an extra line in the output video frame and restarting said accumulating.

34. (original) The method of claim 32, wherein the set of frames has a non-integer average number of lines per frame.

35. (original) The method of claim 28, wherein said generating includes dithering the frequency of the output clock signal to provide a spread spectrum effect.

///